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17CS72

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1   a. Discuss the elements of modern computer systems with diagram. **(10 Marks)**
     b. Consider the execution of an object code with 2,00,000 instructions on a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment :

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60 %
Load / Store	2	18 %
Branch	4	12 %
Memory reference	8	10 %

     i)   Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.
     ii) Calculate the corresponding MIPS rate based on the CPI obtained in part (i). **(10 Marks)**

OR

2   a. Explain the different types of shared memory processors with diagram. **(10 Marks)**
     b. Discuss the various static interconnection networks with bisection width, node degree, diameter and number of links. **(10 Marks)**

Module-2

3   a. Compare the characteristics of CISC & RISC architectures, with the aid diagram. **(10 Marks)**
     b. Explain the architectures of a VLIW (Very Long Instruction Word) processor and its pipeline operations. **(10 Marks)**

OR

4   a. Draw the architecture of SPARC processor and floating point unit on two separate chips. **(10 Marks)**
     b. Explain the memory page replacement policies used in Virtual Memory Technology. **(10 Marks)**

Module-3

5   a. Explain the Fully – associative cache organisation with mapping examples. **(10 Marks)**
     b. Design a pipeline unit for fixed point multiplication of 8 – bit integers using CSA and CPA. (Carry Save Adder and Carry Propagation Adder). **(10 Marks)**

OR

6 a. Discuss the central and distributed arbitration techniques with the aid of timing diagrams.

(10 Marks)

   b. Consider the following pipeline reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

   i) What are the Forbidden latencies?
   ii) Draw the state transition diagram.
   iii) List all the sample and greedy cycles.
   iv) Determine the optimal constant latency cycle and minimum average latency.
   v) Determine the throughput of the pipeline, if the pipeline clock period be $\tau = 20$ ns.

(10 Marks)

Module-4

7 a. Explain the cache coherence problems in data sharing and in process migration with possible solution. **(10 Marks)**
   b. Describe the architecture of the connection machine – cm – 2 with processor array and processor nodes. **(10 Marks)**

OR

8 a. Compare the static and dynamic data flow computers. Draw the dataflow graph for computing cos x.

$$\cos x \simeq 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!}.$$

(10 Marks)

   b. Explain the three types of cache directory protocols. **(10 Marks)**

Module-5

9 a. Explain the Shared – Variable model of parallel models. **(10 Marks)**
   b. Describe the principles of Synchronization. **(10 Marks)**

OR

10 a. Explain the Tomasulo's Algorithm, with example. **(10 Marks)**
   b. Describe the following :
   i) Reorder Buffer   ii) Register Renaming. **(10 Marks)**

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